ELECTRONIC KITS INTERNATIONAL INC.

STEP BY STEP CONS

(   ) STEP 1

- Check off each Step as you go.
- Use the best quality soldering iron you can (Maximum 60 watts).
- Pick up the circuit board and look at both sides, notice one side has the inscription : "THE MICRO-MENTOR CPU BOARD", the other does not. All the electronic parts in this project will be mounted on the side that has this inscription (component side), and will be soldered to the other side (soldering side). You are now ready to assemble the kit.

(   ) STEP 2

Identify and install the two forty-pin IC sockets, the two sixteen-pin IC sockets and the fourteen-pin IC socket. Solder carefully avoiding solder bridges between pins.

(   ) STEP 3

Using one of the solid wires provided, make and install the two jumper wires shown in the right upper side of the pictorial diagram of the Micro-Mentor CPU Board. Solder and cut off excess leads.

(   ) STEP 4

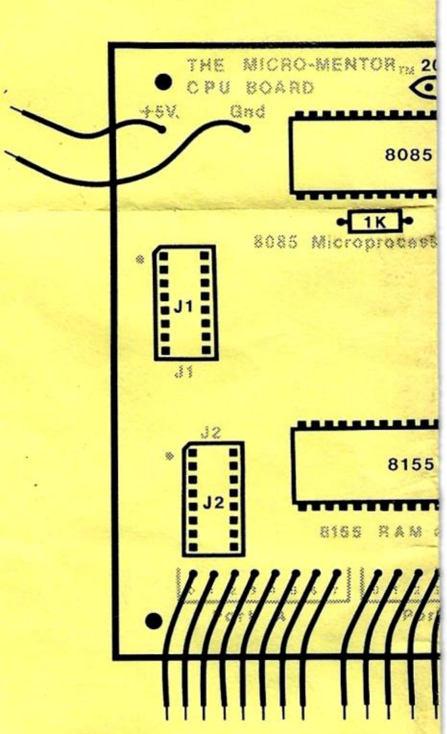
Identify and install the following resistors: the two 1KΩ resistors (Brown, Black, Red, Gold); the two 4.7K Ω resistors (Yellow, Violet, Red, Gold); the 10 KΩ resistor (Brown, Black, Orange, Gold) and the 27 KΩ resistor (Red, Violet, Orange, Gold). Solder and cut off excess leads.

(   ) STEP 5

Identify D1 the 1N4148 diode. Mount it to the circuit board with the band at one end in the correct position, as shown in the pictorial diagram. Solder and cut off excess leads.

CPU B

EKI MICRO-MEN



EKI INC.
MICRO-MENTOR MICRO
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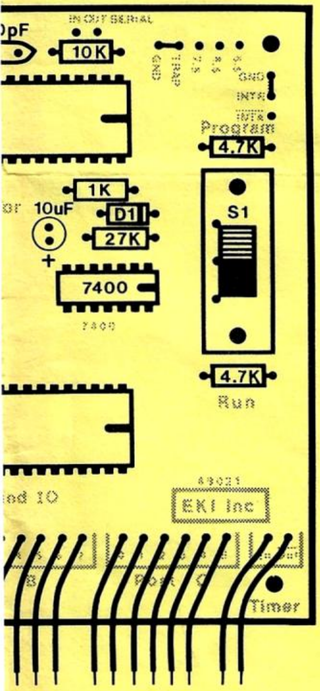
TRUCTION DIAGRAM

OARD
TOR SYSTEM



( ) STEP 6

Identify the 20 pF ceramic capacitor. Install it to the circuit board as shown in the pictorial diagram. Solder and cut off excess leads.

( ) STEP 7

Identify the 10 uF electrolytic capacitor. Mount it to the circuit board with the negative and positive lead in the correct direction, as shown in the pictorial diagram. Solder and cut off excess leads.

( ) STEP 8

Identify S1, the single-pole double-throw switch. Mount it to the circuit board, as shown in the pictorial diagram. Solder and cut off excess leads.

( ) STEP 9

Solder a red wire for the positive supply to the hole marked "+5V" on the circuit board, and a black wire for the negative to the hole marked "Gnd". Cut off excess leads.

( ) STEP 10

Install the three IC's (8085, 8155 and 7400) on the sockets, as shown in the pictorial diagram, with the notch or band in the correct direction.

( ) STEP 11

Solder the 24 solid wires to the port and timer outputs, as shown in the pictorial diagram. Cut off excess leads.

PROCESSOR SYSTEM.
c Kits International, Inc.

ELECTRONIC KITS INTERNATIONAL INC.

STEP BY STEP CONST

( ) STEP 1

- Check off each step as you go.
- Use the best quality soldering iron you can (maximum 60 watts).
- Pick up the circuit board and look at both sides, notice one side has the inscription "MICRO - MENTOR KEYBOARD PROGRAMMER", the other does not. All the electronic parts in this project will be mounted on the side that has this inscription (component side), and will be soldered to the other side (soldering side). You are now ready to assemble the kit.

( ) STEP 2

Identify and installl the five sixteen-pin IC sockets, the three fourteen-pin IC sockets and the eighteen-pin IC socket. Solder carefully avoiding solder bridges between pins.

( ) STEP 3

Identify the eight LED's. Mount them to the circuit board with the flat side (shorter lead) in the correct direction, as shown in the pictorial diagram. Leave about 1/8 to 1/4 inch between the bodies of the LED's and the surface of the circuit board. Solder and cut off excess leads.

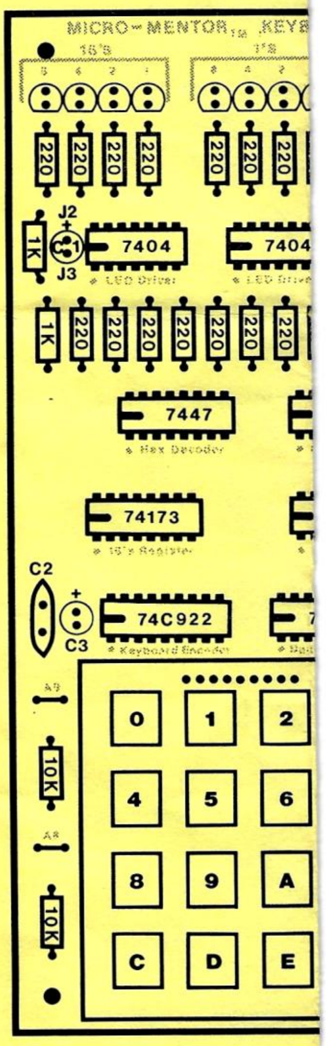
( ) STEP 4

Identify the double seven-segment display. Mount it to the circuit board (Please note, will fit in only one direction). Solder the pins carefully avoiding solder bridges and cut off excess leads.

( ) STEP 5

Identify and install the following resistors: the twenty-two 220 Ω resistors (Red, Red, Brown, Gold); the two 1KΩ resistors (Brown, Black, Red, Gold); the two 1.2 KΩ resistors (Brown, Red, Red, Gold); the three 10KΩ resistors (Brown, Black, Orange, Gold); the two 47 KΩ resistors (Yellow, Violet, Orange, Gold) and the 2.2 KΩ resistor (Red, Red, Red, Gold).
Solder and cut off excess leads.

KEYBOARD PROG
EKI MICRO-MEN



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MICRO-MENTOR MICR
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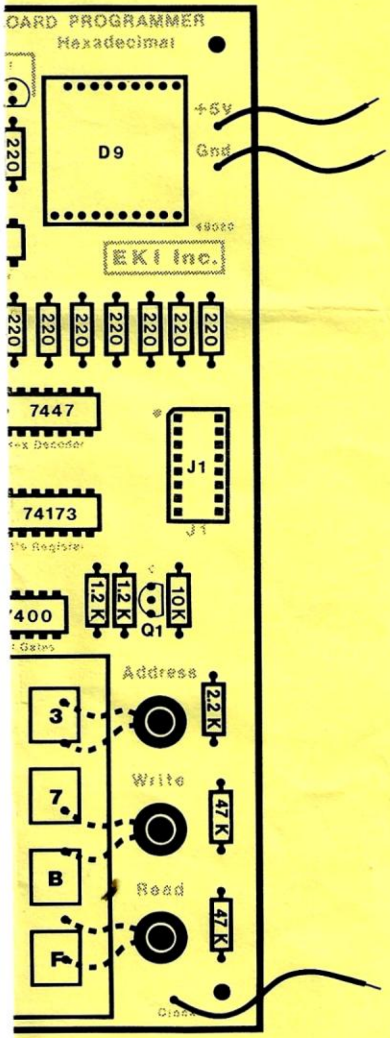
RUCTION DIAGRAM

RAMMER BOARD
TOR SYSTEM



PROCESSOR SYSTEM.
nic Kits International, Inc.

( ) **STEP 6**

Identify C1, the 3.3 uF electrolytic capacitor and C3, the 1uF electrolytic capacitor. Mount them to the circuit board with the negative and positive lead in the correct direction, as shown in the pictorial diagram. Solder and cut off excess leads.

( ) **STEP 7**

Identify C2, the .1 uF ceramic capacitor (this capacitor may be marked: .1 or 104). Mount it to the circuit board, as shown in the pictorial diagram. Solder and cut off excess leads.

( ) **STEP 8**

Using one of the solid wires provided, make and install the two jumper wires (A8 and A9) shown in the lower left side of the pictorial diagram of the Micro-Mentor Programmer board.

( ) **STEP 9**

Find the keyboard and install it to the circuit board as shown in the pictorial diagram. Solder and cut off excess leads.

( ) **STEP 10**

Find Q1, the 2N3904 transistor. Install it in the circuit board with the flat side in the correct direction, as shown in the pictorial diagram.

( ) **STEP 11**

Identify the three push-button switches. Mount them from the soldering side of the board and screw the metal nut on the top side of the board. Solder wires from the legs of the switches to the circuit board, as shown in the pictorial diagram.

( ) **STEP 12**

Solder a red wire for the positive supply to the hole marked "+5V" on the circuit board, and a black wire for the negative, to the hole marked "Gnd". Cut off excess leads.

( ) **STEP 13**

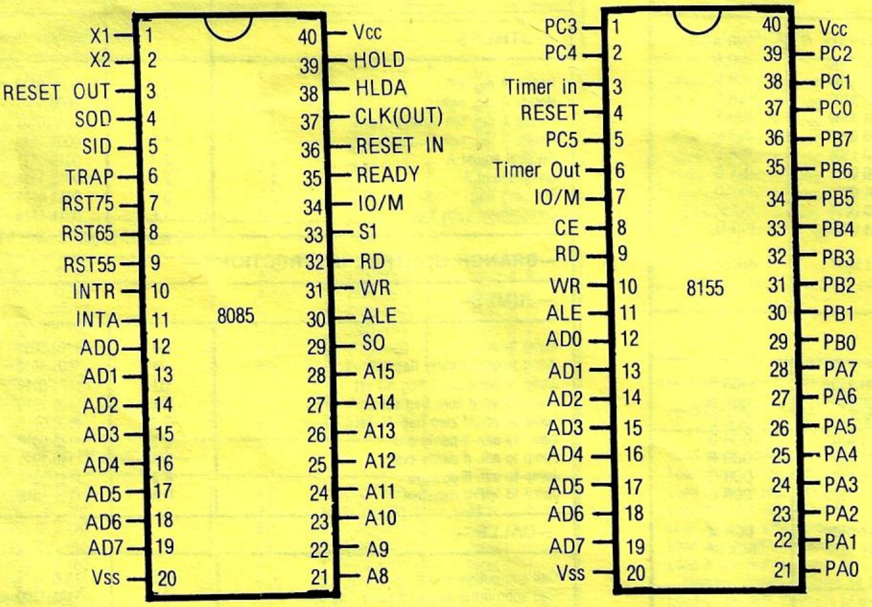
Solder a black solid wire to the hole marked "Clock", shown on the lower right side of the pictorial diagram of the programmer board.

( ) **STEP 14**

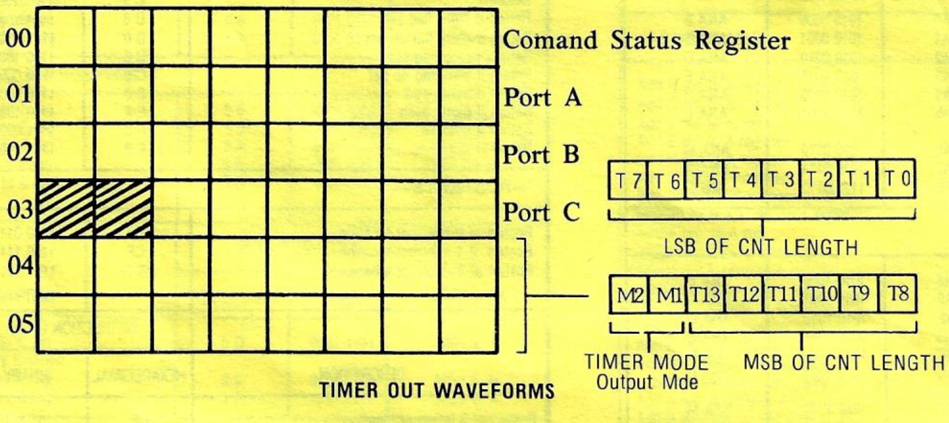
Find the eight IC's. Insert them in their respective sockets with the notch or band in the correct direction, as shown in the pictorial diagram.

PROGRAMMER'S GUIDE FOR THE E

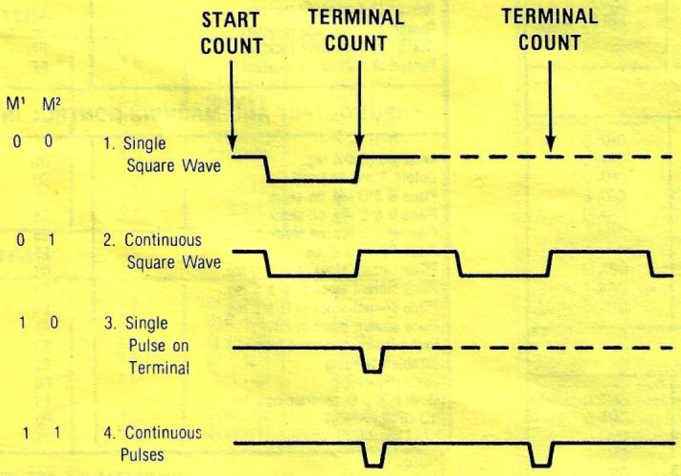
PIN-OUT OF THE 8085 AND 8155



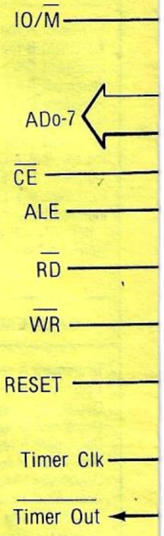
REGISTERS OF THE 8155



TIMER OUT WAVEFORMS


START COUNT
TERMINAL COUNT
TERMINAL COUNT
M1 M2
0 0 1. Single Square Wave
0 1 2. Continuous Square Wave
1 0 3. Single Pulse on Terminal
1 1 4. Continuous Pulses

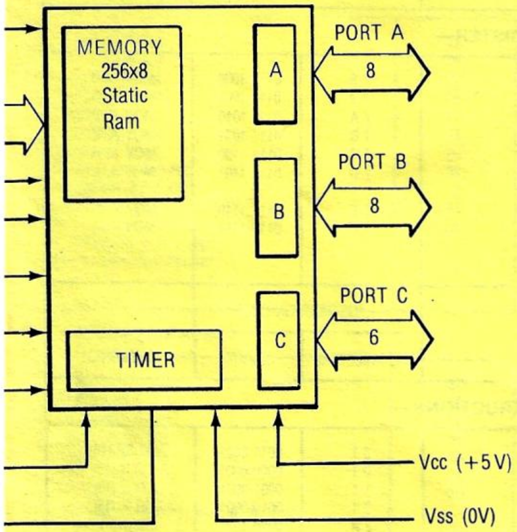
8155



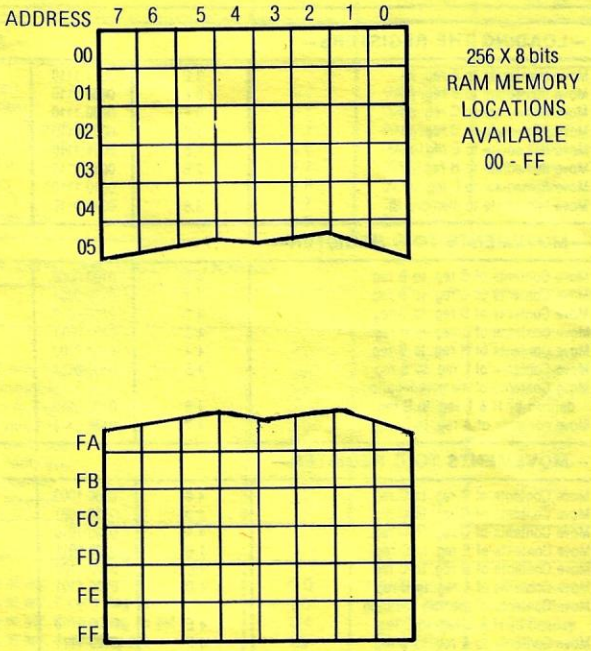
COMMA

KI MICRO-MENTOR T.M. SYSTEM

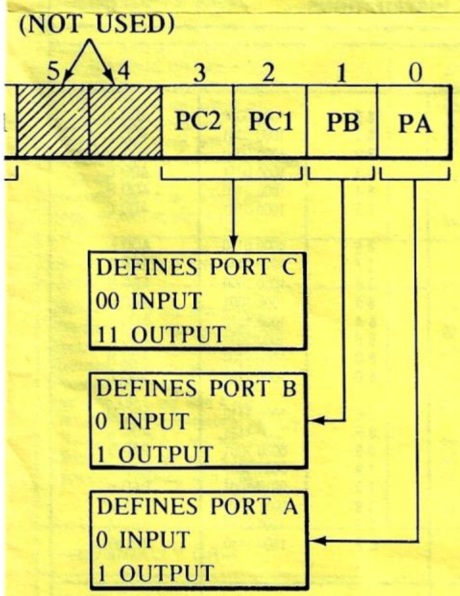
BLOCK DIAGRAM



MEMORY MAP



ND STATUS REGISTER



LS TIMER
FFECT
TIMER IMMEDIATELY
TIMER WHEN ZERO IS REACHED
T TIMER OR RESTART AFTER ZERO
ACHED

HEXADECIMAL/BINARY CONVERSION CHART

Hexadecimal Digit	Binary Equivalent	Symbol shown on 7-Segment display
0	0000	0
1	0001	1
2	0010	2
3	0011	3
4	0100	4
5	0101	5
6	0110	6
7	0111	7
8	1000	8
9	1001	9
A	1010	⊏
B	1011	⊐
C	1100	⊔
D	1101	⊑
E	1110	⊢
F	1111	BLANK

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MICRO-MENTOR MICROPROCESSOR SYSTEM
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EKI PROGRAMMING INSTRUCTION SET FOR 8085

DESCRIPTION	INSTRUCTION CODE		MNEMONIC
	HEXADECIMAL	BINARY	
—DATA TRANSFER INSTRUCTIONS—			
—LOADING THE REGISTERS—			
Move Immediate to A reg. (8)	3 E	0011 1110	MVI A, (8)
Move Immediate to B reg. (8)	0 6	0000 0110	MVI B, (8)
Move Immediate to C reg. (8)	0 E	0000 1110	MVI C, (8)
Move Immediate to D reg. (8)	1 6	0001 0110	MVI D, (8)
Move Immediate to E reg. (8)	1 E	0001 1110	MVI, E. (8)
Move Immediate to H reg. (8)	2 6	0010 0110	MVI H, (8)
Move Immediate to L reg. (8)	2 E	0010 1110	MVI L, (8)
Move Immediate to memory (8)	3 6	0011 0110	MVI M, (8)
—MOVEMENTS TO B REGISTER—			
Move Contents of B reg. to B reg.	4 0	0100 0000	MOV B, B
Move Contents of C reg. to B reg.	4 1	0100 0001	MOV B, C
Move Contents of D reg. to B reg.	4 2	0100 0010	MOV B, D
Move Contents of E reg. to B reg.	4 3	0100 0011	MOV B, E
Move Contents of H reg. to B reg.	4 4	0100 0100	MOV B, H
Move Contents of L reg. to B reg.	4 5	0100 0101	MOV B, L
Move Contents of memory location defined by H & L reg. to B reg.	4 6	0100 0110	MOV B, M
Move contents of A reg. to B reg.	4 7	0100 0111	MOV B, A
—MOVEMENTS TO C REGISTER—			
Move Contents of B reg. to C reg.	4 8	0100 1000	MOV C, B
Move Contents of C reg. to C reg.	4 9	0100 1001	MOV C, C
Move Contents of D reg. to C reg.	4 A	0100 1010	MOV C, D
Move Contents of E reg. to C reg.	4 B	0100 1011	MOV C, E
Move Contents of H reg. to C reg.	4 C	0100 1100	MOV C, H
Move Contents of L reg. to C reg.	4 D	0100 1101	MOV C, L
Move Contents of memory location defined by H & L reg. to C reg.	4 E	0100 1110	MOV, C, M
Move Contents to A reg. to C reg.	4 F	0100 1111	MOV C, A
—MOVEMENTS TO D REGISTER—			
Move Contents of B reg. to D reg.	5 0	0101 0000	MOV D, B
Move Contents of C reg. to D reg.	5 1	0101 0001	MOV D, C
Move Contents of D reg. to D reg.	5 2	0101 0010	MOV D, D
Move Contents of E reg. to D reg.	5 3	0101 0011	MOV D, E
Move Contents of H reg. to D reg.	5 4	0101 0100	MOV D, H
Move Contents of L reg. to D reg.	5 5	0101 0101	MOV D, L
Move contents of memory location defined by H & L reg. to D reg.	5 6	0101 0110	MOV D, M
Move contents of A reg. to D reg.	5 7	0101 0111	MOV D, A
—MOVEMENTS TO E REGISTER—			
Move contents of B reg. to E reg.	5 8	0101 1000	MOV E, B
Move contents of C reg. to E reg.	5 9	0101 1001	MOV E, C
Move contents of D reg. to E reg.	5 A	0101 1010	MOV E, D
Move contents of E reg. to E reg.	5 B	0101 1011	MOV E, E
Move contents of H reg. to E reg.	5 C	0101 1100	MOV E, H
Move contents of L reg. to E reg.	5 D	0101 1101	MOV E, L
Move contents of memory location defined by H & L reg. to E reg.	5 E	0101 1110	MOV E, M
Move contents of A reg. ro E reg.	5 F	0101 1111	MOV E, A
—MOVEMENTS TO H REGISTER—			
Move contents of B reg. to H reg.	6 0	0110 0000	MOV H, B
Move contents of C reg. to H reg.	6 1	0110 0001	MOV H, C
Move contents of D reg. to H reg.	6 2	0110 0010	MOV H, D
Move contents of E reg. to H reg.	6 3	0110 0011	MOV H, E
Move contents of H reg. to H reg.	6 4	0110 0100	MOV H, H
Move contents of L reg. to H reg.	6 5	0110 0101	MOV H, L
Move contents of memory location defined by H & L reg. to H reg.	6 6	0110 0110	MOV H, M
Move contents of A reg. to H reg.	6 7	0110 0111	MOV H, A
—MOVEMENTS TO L REGISTER—			
Move contents of B reg. to L reg.	6 8	0110 1000	MOV L, B
Move contents of C reg. to L reg.	6 9	0110 1001	MOV L, C
Move contents of D reg. to L reg.	6 A	0110 1010	MOV L, D
Move contents of E reg. to L reg.	6 B	0110 1011	MOV L, E
Move contents of H reg. to L reg.	6 C	0110 1100	MOV L, H
Move contents of memory location defined by H & L reg. to L reg.	6 E	0110 1110	MOV L, M
Move contents of A reg. to L reg.	6 F	0110 1111	MOV L, A
—MOVEMENTS FROM REGISTERS TO MEMORY—			
Move contents of B reg. to memory*	7 0	0111 0000	MOV M, B
Move contents of C reg. to memory*	71	0111 0001	MOV M, C
Move contents of D reg. to memory*	7 2	0111 0010	MOV M, D
Move contents of E reg. to memory*	73	0111 0011	MOV M, E
Move contents of H reg. to memory*	74	0111 0100	MOV M, H
Move contents of L reg. to memory*	7 5	0111 0101	MOV M, L
Move contents of A reg. to memory*	7 7	0111 0111	MOV M, A
*The address of the memory location is defined by the cotents of H & L reg.			
—MOVEMENTS TO A REGISTER—			
Move contents of B reg. to A reg.	7 8	0111 1000	MOV A, B
Move contents of C reg. to A reg.	7 9	0111 1001	MOV A, C
Move contents of D reg. to A reg.	7 A	0111 1010	MOV A, D
Move contents of E reg. to A reg.	7 B	0111 1011	MOV A, E
Move contents of H reg. to A reg.	7 C	0111 1100	MOV A, H
Move contents of L reg. to A reg.	7 D	0111 1101	MOV A, L
More contents of memory location defined by H & L reg. to A reg.	7 E	0111 1110	MOV A, M
Move contents of A reg. to A reg.	7 F	0111 1111	MOV A, A
—STORE AND LOAD INSTRUCTIONS—			
Load stack pointer with (16)	3 1	0011 0001	LXI SP (16)
Load B and C reg. with (16)	0 1	0000 0001	LXI B (16)
Load D and E reg. with (16)	1 1	0001 0001	LXI D (16)
Load H and L reg. with (16)	2 1	0010 0001	LXI H (16)
Load H and L with contents of adr.	2 A	0010 1010	LHLD Adr.
Load A reg. with contents of adr.	3 A	0011 1010	LDA Adr.
Load A reg. with contents of memory location defined by B & C reg.	0 A	0000 1010	LDAX B
Load A reg. with contents of memory location defined by D & E reg.	1 A	0001 1010	LDAX D
Store A reg. in memory location by B & C reg.	0 2	0000 0010	STAX B
Store A reg. in memory location defined by D & E reg.	1 2	0001 0010	STAX D
Store A in adr.	3 2	0011 0010	STA Adr.
Store H & L in adr and adr.+ 1	2 2	0010 0010	SHLD Adr.
Move H & L to stack pointer	F 9	1111 1001	SPHL
—ARITHMETICAL AND LOGICAL INSTRUCTIONS—			
—ADDITIONS—			
Add B reg to A register	8 0	1000 0000	ADD B
Add C reg to A register	8 1	1000 0001	ADD C
Add D reg to A register	8 2	1000 0010	ADD D
Add E reg to A register	8 3	1000 0011	ADD E
Add H reg to A register	8 4	1000 0100	ADD H
Add L reg to A register	8 5	1000 0101	ADD L
Add contents of memory location defined by H & L reg. to A register	8 6	1000 0110	ADD M
Add A reg. to A reg.	8 7	1000 0111	ADD A
Add B reg & carry to A reg	8 8	1000 1000	ADC B
Add C reg & carry to A reg	8 9	1000 1001	ADC C
Add D reg & carry to A reg	8 A	1000 1010	ADC D
Add E reg & carry to A reg	8 B	1000 1011	ADC E
Add H reg & carry to A reg	8 C	1000 1100	ADC H
Add L reg & carry to A reg	8 D	1000 1101	ADC L
Add contents of memory location defined by H & L and carry to A reg.	8 E	1000 1110	ADC M
Add A reg. & carry to A reg.	8 F	1000 1111	ADC A
Add B & C reg. to H & L Reg.	0 9	0000 1001	DAD B
Add D & E reg. to H & L Reg.	1 9	0001 1001	DAD D
Add H & L reg. to H & L Reg.	2 9	0010 1001	DAD H
Add stock pointer to H & L reg.	3 9	0011 1001	DAD SP
Add (8) to A reg.	C 6	1100 0110	ADI (8)
Add (8) & carry to A reg.	C E	1100 1110	ACI (8)
—SUBTRACTIONS—			
Subtract B reg. from A reg.	90	1001 0000	SUB B
Subtract C reg. from A reg.	91	1001 0001	SUBC
Subtract D reg. from A reg.	92	1001 0010	SUB D
Subtract E reg. from A reg.	93	1001 0011	SUB E
Subtract H reg. from A reg.	94	1001 0100	SUB H
Subtract L reg. from A reg.	95	1001 0101	SUB L
Subtract contents of memory loc. def. by H & L reg. from A reg.	96	1001 0110	SUM M
Subtract A reg. from A reg.	97	1001 0111	SUB A
Sub. B reg. and borrow from A reg.	98	1001 1000	SBB B
Sub. C reg. and borrow from A reg.	99	1001 1001	SBB C
Sub. D reg. and borrow from A reg.	9A	1001-1010	SBB D
Sub. E reg. and borrow from A reg.	9B	1001 1011	SBB E
Sub. H reg. and borrow from A reg.	9C	1001 1100	SBB H
Sub. L reg. and borrow from A reg.	9D	1001 1101	SBB L

CRO-MENTOR T.M. MICROPROCESSOR SYSTEM

Sub. contents of memory Loc. def by H & L and borrow from A reg.	9E	1001 1110	SBB M
Sub. A reg. and borrow from A reg.	9F	1001 1111	SBB A
Subtract (8) from A reg.	D6	1101-0110	SUI (8)
Sub. (8) and borrow from A reg.	DE	1101 1110	SBI (8)
—INCREMENTS—			
Increment A reg.	3C	0011 1100	INR A
Increment B reg.	04	0000 0100	INR B
Increment C reg.	0C	0000 1100	INR C
Increment D reg.	14	0001 0100	INR D
Increment E reg.	1C	0001 1100	INR E
Increment H reg.	24	0010 0100	INR H
Increment L reg.	2C	0010 1100	INR L
Increment B & C reg.	03	0000 0011	INX B
Increment D & E reg.	13	0001 0011	INX D
Increment H & L reg.	23	0010 0011	INX H
Increment the memory location defined by H & L reg.	34	0011 0100	INR M
Increment Stock Pointer	33	0011 0011	INX SP
—DECREMENTS—			
Decrement A reg.	3D	0011 1101	DCR A
Decrement B reg.	05	0000 0101	DCR B
Decrement C reg.	0D	0000 1101	DCR C
Decrement D reg.	15	0001 0101	DCR D
Decrement E reg.	1D	0001 1101	DCR E
Decrement H reg.	25	0010 0101	DCR H
Decrement L reg.	2D	0010 1101	DCR L
Decrement memory location defined by H & L reg.	35	0011 0101	DCR M
Decrement Stock Pointer	3B	0011 1011	DCX SP

DESCRIPTION	INSTRUCTION CODE		MNEMONIC
	HEXADECIMAL	BINARY	
Decrement B & C reg.	0B	0000 1011	DCX B
Decrement D & E reg.	1B	0001 1011	DCX D
Decrement H & L reg.	2B	0010 1011	DCX H
—LOGICALLY AND—			
Logically AND B reg. with A reg.	A0	1010 0000	ANA B
Logically AND C reg. with A reg.	A1	1010 0001	ANA C
Logically AND D reg. with A reg.	A2	1010 0010	ANA D
Logically AND E reg. with A reg.	A3	1010 0011	ANA E
Logically AND H reg. with A reg.	A4	1010 0100	ANA H
Logically AND L reg. with A reg.	A5	1010 0101	ANA L
Logically AND the contents of memory loc def by H & L reg. with A reg.	A6	1010 0110	ANA M
Logically AND A reg. with A reg.	A7	1010 0111	ANA A
Logically AND (8) with A reg.	E6	1110 0110	ANI 8
—EXCLUSIVE OR—			
Exclusive OR B reg. with A reg.	A8	1010 1000	XRA B
Exclusive OR C reg. with A reg.	A9	1010 1001	XRA C
Exclusive OR D reg. with A reg.	AA	1010 1010	XRA D
Exclusive OR E reg. with A reg.	AB	1010 1011	XRA E
Exclusive OR H reg. with A reg.	AC	1010 1100	XRA H
Exclusive OR L reg. with A reg.	AD	1010 1101	XRA L
Exclusive OR the contents of memory loc. def. by H & L reg. with A reg.	AE	1010 1110	XRA M
Exclusive OR A reg. with A reg.	AF	1010 1111	XRA A
Exclusive OR (8) reg. with A reg.	EE	1010 1010	XRI 8
—LOGICALLY OR—			
Logically OR B reg. with A reg.	B0	1011 0000	ORA B
Logically OR C reg. with A reg.	B1	1011 0001	ORA C
Logically OR D reg. with A reg.	B2	1011 0010	ORA D
Logically OR E reg. with A reg.	B3	1011 0011	ORA E
Logically OR H reg. with A reg.	B4	1011 0100	ORA H
Logically OR L reg. with A reg.	B5	1011 0101	ORA L
Logically OR memory loc. defined by H & L reg. with A reg.	B6	1011 0110	ORA M
Logically OR A reg. with A reg.	B7	1011 0111	ORA A
Logically OR (8) reg. with A reg.	F6	1111 0110	ORI (8)
—COMPARE—			
Compare B reg. with A reg.	B8	1011 1000	CMP B
Compare C reg. with A reg.	B9	1011 1001	CMP C
Compare D reg. with A reg.	BA	1011 1010	CMP D
Compare E reg. with A reg.	BB	1011 1011	CMP E
Compare H reg. with A reg.	BC	1011 1100	CMP H
Compare L reg. with A reg.	BD	1011 1101	CMP L
Compare contents of memory loc. def. by H & L reg. with A reg.	BE	1011 1110	CMP M
Compare A reg. with A reg.	BF	1011 1111	CMP A

DESCRIPTION	INSTRUCTION CODE		MNEMONIC
	HEXADECIMAL	BINARY	
Compare (8) with A reg.	F E	1111 1110	CPI (8)
—OTHERS—			
Rotate A reg. left	0 7	0000 0111	RLC
Rotate A reg. right	0 F	0000 1111	RRC
Rotate A reg. left through carry	1 7	0001 0111	RAL
Rotate A reg. righ through carry	1 F	0001 1111	RAR
Decimal adjust A	2 7	0010 0111	DAA
Complement A	2 F	0010 1111	CMA
Set carry flag	3 7	0011 0111	STC
Complement carry flag	3 F	0011 1111	CMC
—BRANCH CONTROL INSTRUCTIONS—			
—JUMPS—			
Jump to adr.	C3	1100 0011	JMP (Adr.)
Jump to adr. if carry flag set	DA	1101 1010	JC (adr.)
Jump to adr.if carry flag no set	D2	1101 0010	JNC (adr.)
Jump to adr.if zero flag set	CA	1100 1010	JZ (adr.)
Jump to adr. if zero flag no set	C 2	1100 0010	JNZ (Adr.)
Jump to adr. if parity odd	E 2	1110 0010	JPO (adr.)
Jump to adr. if parity even	E A	1110 1010	JPE (adr.)
Jump to adr. if positive	F 2	1111 0010	JP (adr.)
Jump to adr. if negative	F A	1111 1010	JM (adr.)
—CALLS—			
Call subroutine at adr.	C D	1100 1101	CALL (adr.)
Call subroutine at adr. if carry flag set	DC	1101 1100	CC (adr.)
Call subroutine at adr. if carry flag no set	D 4	1101 0100	CNC (adr.)
Call subroutine at adr. if zero flag set	CC	1100 1100	CZ (adr.)
Call subroutine at adr. if zero flag no set	C 4	1100-0100	CNZ (adr.)
Call subroutine at adr. if parity odd	E 4	1110 0100	CPO (adr.)
Call subroutine at adr. if parity even	E C	1110 1100	CPE (adr.)
Call subroutine at adr. if positive	F 4	1111 0100	CP (adr.)
Call subroutine at adr. if negative	F C	1111 1100	CM (adr.)
—RETURNS—			
Return	C 9	1100 1001	RET
Return if carry flag set	D 8	1101 1000	RC
Return if carry flaf no set	D 0	1101 0000	RNC
Return if zero flag set	C 8	1100 1000	RZ
Return if zero flag no set	C 0	1100 0000	RNZ
Return if parity odd	E 0	1110 0000	RPO
Return if parity even	E 8	1110 1000	RPE
Return if positive	F 0	1111 0000	RP
Return if negative	F 8	1111 1000	RM
—RESTARTS—			
Restart at 0 interrupt location	C7	1100 0111	RST 0
Restart at 1 interrupt location	CF	1100 1111	RST 1
Restart at 2 interrupt location	D 7	1101 0111	RST 2

DESCRIPTION	INSTRUCTION CODE		MNEMONIC
	HEXADECIMAL	BINARY	
Restart at 3 interrupt location	DF	1101 1111	RST 3
Restart at 4 interrupt location	E7	1110 0111	RST 4
Restart at 5 interrupt location	EF	1110 1111	RST 5
Restart at 6 interrupt location	F7	1111 0111	RST 6
Restart at 7 interrupt location	FF	1111 1111	RST 7
—INPUT/OUTPUT AND MACHINE CONTROL INSTRUCTIONS—			
Input (port) to A reg.	DB	1101 1011	IN (port)
Output A reg. to (port)	D3	1101 0011	Out (port)
Place B & C reg. on stock	C5	1100 0101	PUSH B
Place D & E reg. on stock	D5	1101 0101	PUSH D
Place H & L reg. on stock	E5	1110 0101	PUSH H
Place PSW on stock	F5	1111 0101	PUSH PSW
Place current stock in B & C reg.	C1	1100 0001	POP B
Place current stock in D & E reg.	D1	1101 0001	POP D
Place current stock in H & L reg.	E1	1110 0001	POP H
Place current stock in PSW	F1	1111 0001	POP PSW
Exchange current stock with H & L	E3	1110 0001	XTHL
Disable interrupts	F3	1111 0011	DI
Enable interrupts	FB	1111 1011	EI
Move H & L to program counter	E9	1110 1001	PCHL
NO OPPERATION	00	0000 0000	NOP
HALT machine operation	76	0111 0110	HALT

Notes:

(adr.): Three byte instruction requiring an address as bytes 2 & 3

(8): Two byte instruction requiring on 8 bit data word.

(16): Three byte instruction requiring two 8 bit data words.

EKI, INC. MICRO-MENTOR MICROPROCESSOR SYSTEM